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10/586,690	07/20/2006	Tadatomo Suga	YANE-0003-US1	6233

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EXAMINER	
PATEL, DEVANG R	
ART UNIT	PAPER NUMBER
1793	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,690	SUGA ET AL.	
	Examiner	Art Unit	
	DEVANG PATEL	1793	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-59* is/are pending in the application.

4a) Of the above claim(s) *21 and 26-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-20,22-25 and 50-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. **Claims 25, 51 and 54-58** are rejected under 35 U.S.C. 102(a) as being anticipated by Yamauchi (WO 2003/001858 A1, of record). US 2004/0169020 is taken to be English-language equivalent of WO 2003001858 A1 and sections pointed out in the rejection below refer to the US publication.

a. **Regarding claim 51, Yamauchi** discloses a bonding method (fig. 1; ¶ 8-11) for bonding objects to be bonded (chip 2 and substrate 3) which have a bonding portion (4, 5) formed of a metal, wherein the bonding portions are gold/gold bonding, which inherently have a hardness of 200 Hv or less. The bonding portions are contacted with each other and pressed in a solid phase at low temperature of about 150 ºC (meets the claimed range from room temperature to 180 ºC) after treating the bonding portions with plasma (¶ 142-143). Each of the objects (chip 2 and substrate 3) includes at least one material other than gold.

b. **Claims 25 and 54-57** are product-by-process claims since they claim a semiconductor device or the like (product) formed by a previously recited bonding method. Even though product-by-process claims are limited by and

defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production *(See MPEP 2113)*. Therefore, these claims are met by Yamauchi.

c. **As to claim 58,** Yamauchi discloses that the bonding portion is formed in the shape of a contour, said bonding portion is surface-activated with said energy wave, and thereafter, said objects to be bonded are bonded together in a solid phase at room temperature, so that space surrounded in said shape of contour by said bonding portions is formed between said bonding surfaces of said objects to be bonded to enclose a predetermined atmosphere in said space.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 2, 5-6, 8, 15, 17, 19, 22-25 and 50** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gosele et al. (Applied Physics Letters, 1995) in view of Takagi et al. (Applied Physics Letters, 1999) and further in view of Yamauchi (WO 2003/001858 A1, of record).

a. **Regarding claim 2**, Gosele et al. ("**Gosele**") discloses a bonding method for bonding objects (Si wafers) by treating Si wafers in HF acid to etch away native oxide layer (pg. 863- ¶ 3) and then contacting the wafers in atmospheric

air under pressure varying between 10 and 10^5 Pa (pg. 864- ¶ 2). In accordance with broadest reasonable interpretation, the limitation *"low vacuum of 10^{-5} torr or more in atmospheric air"* includes pressure ranging from vacuum of 10^{-5} torr to atmospheric pressure (760 torr), and thus, the pressure disclosed by Gosele (0.075-75 torr) meets the claimed range. Gosele discloses crushing an adhering oxide layer (SiO_2) by pressing the wafers to be bonded at room temperature (fig. 1). It is also noted that adhering oxide/substance layer would intrinsically form on the bonding surfaces since bonding is performed in atmospheric air (present specification - pg. 4, ¶ 3).

b. Gosele discloses etching treatment but does not expressly mention an energy wave treatment. However, such technique is well-known in the art. **Takagi** et al. (directed to room-temperature bonding of silicon wafer) teaches etching the surfaces of bonding specimens by argon beam in vacuum to remove contaminants thereby activating the surfaces. Takagi further teaches that such surface-activated bonding (SAB) method has been applied to Si-Si bonding (pg. 2387- ¶ 3). In view of that, it would have been obvious to a person of ordinary skill in the art at the time of the invention to etch the bonding surfaces by an energy beam treatment in the method of Gosele since such is an art-recognized alternative technique of cleaning bonding surfaces.

c. Neither Gosele nor Takagi teaches bonding portions formed of gold. However, **Yamauchi** (drawn to room-temperature chip bonding after plasma treatment) discloses bonding objects (including wafer- ¶ 135), wherein the

bonding portions (bumps 4 and pads 5- gold/gold bonding) are contacted with each other and pressed in a solid phase at low temperature of about 150 ºC after activating the bonding surfaces by treating with plasma (¶ 142-143). The wafer objects (chip or substrate- ¶ 135) of Yamauchi are analogous to Si wafers of Gosele. It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide gold bonding portions similar to Yamauchi in the method Gosele in order to produce a desired semiconductor device. In addition, one skilled in the art would have been motivated to implement SAB technique for joining gold solder bumps on substrate because doing so allows room-temperature bonding, which reduces costs and time associated with conventional heating.

d. **As to claim 5,** Yamauchi discloses various energy wave cleaning techniques such as ion beam, atomic beam (similar to Takagi), plasma, radical beam or laser (¶ 17). In view of that, it would have been obvious to a person of ordinary skill in the art at the time of the invention to etch the bonding surfaces by a low-pressure plasma treatment in the method of Gosele since such is an art-recognized alternative technique of cleaning bonding surfaces.

e. **As to claim 6,** Yamauchi discloses that low-pressure plasma for cleaning is generated with electric field having alternating + and - directions generated by an alternating power supply 11/25/150 (figs. 1-4, 16-18). In view of that, it would have been obvious to a person of ordinary skill in the art at the time of the

invention to employ alternating power supply of Yamauchi in the bonding method of Gosele since such is art-recognized technique for plasma generation.

f. **As to claim 8,** in accordance with broadest reasonable interpretation, the oscillating power supply of Yamauchi in the method of Gosele (as explained in claim 6 above) is equivalent to a wave generating power supply capable of controlling a pulse width.

g. **As to claim 15,** Gosele in view of Takagi and Yamauchi discloses that the bonding portion is formed in the shape of a contour, said bonding portion is surface-activated with said energy wave, and thereafter, said objects to be bonded are bonded together in a solid phase at room temperature, so that space surrounded in said shape of contour by said bonding portions is formed between said bonding surfaces of said objects to be bonded to enclose a predetermined atmosphere in said space.

h. **As to claim 17,** Gosele discloses that room-temperature bonding is performed in a vacuum (pressure below atmospheric).

i. **As to claim 19**, Gosele discloses bonding in atmospheric air.

j. **As to claim 22,** Yamauchi discloses the objects to be bonded are a chip and a wafer (substrate) (¶ 135). It is known in the art to continuously bond plurality of wafers at room-temperature after energy wave treatment. The claim would have been obvious because continuously bonding plurality of chips to a wafer was recognized as part of ordinary capabilities of one skilled in the art and

would have yielded the predictable result of forming desired semiconductor device.

k. **As to claim 23,** Yamauchi discloses that after predetermined time (in cleaning chamber), chips 2 and substrate 3 are conveyed and simultaneously treated again by energy wave immediately before bonding (¶ 147). It would have been obvious to a person of ordinary skill in the art at the time of the invention to treat the bonding surfaces again with the energy wave in the method of Gosele in order to provide sufficient activated surfaces to allow room-temperature bonding.

l. **As to claims 24-25,** Gosele as modified by Takagi and Yamauchi above includes a semiconductor device (IC chip 2).

m. **Regarding claim 50, Gosele** discloses a bonding method for bonding objects (Si wafers) by treating Si wafers in HF acid to etch away native oxide layer (pg. 863- ¶ 3) and then contacting the wafers in atmospheric air under pressure varying between 10 and 10^5 Pa (pg. 864- ¶ 2). In accordance with broadest reasonable interpretation, the recited low vacuum of 10^{-5} torr or more in atmospheric air includes pressure ranging from vacuum of 10^{-5} torr to atmospheric pressure (760 torr), and thus, the pressure disclosed by Gosele (0.075-75 torr) meets the claimed range. Gosele discloses crushing an adhering oxide layer (SiO_2) by pressing the wafers to be bonded at room temperature (fig. 1). It is also noted that adhering oxide/substance layer would intrinsically form on the bonding surfaces since bonding is performed in atmospheric air.

n. Gosele discloses etching treatment but does not expressly mention an energy wave treatment. However, such technique is well-known in the art. **Takagi** et al. (directed to room-temperature bonding of silicon wafer) teaches etching the surfaces of bonding specimens by Ar beam in vacuum to remove contaminants thereby activating the surfaces. Takagi further teaches that such surface-activated bonding (SAB) method has been applied to Si-Si bonding (pg. 2387- ¶ 3). **Yamauchi** (drawn to room-temperature chip bonding after plasma treatment) discloses various energy wave cleaning techniques such as ion beam, atomic beam (similar to Takagi), plasma, radical beam or laser (¶ 17). In view of collective disclosures of Takagi and Yamauchi, it would have been obvious to a person of ordinary skill in the art at the time of the invention to etch the bonding surfaces by a plasma treatment in the method of Gosele since such is an art-recognized alternative technique of cleaning bonding surfaces.

o. Neither Gosele nor Takagi teaches bonding portions formed of gold. However, **Yamauchi** discloses bonding objects (including wafer- ¶ 135), wherein the bonding portions (bumps 4 and pads 5- gold/gold bonding) are contacted with each other and pressed in a solid phase at low temperature of about 150 ºC after activating the surfaces by treating the bonding portions with plasma (¶ 142-143). The gold bonding portions inherently have a hardness value of 20 Hv to 200 Hv. The wafer objects (chip or substrate- ¶ 135) of Yamauchi are analogous to Si wafers of Gosele. It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide gold bonding portions similar to

Yamauchi in the method Gosele in order to produce a desired semiconductor device. In addition, one skilled in the art would have been motivated to implement SAB method for joining gold solder bumps on substrate because doing so allows room-temperature bonding, which reduces costs and time associated with conventional heating.

5. **Claims 3-4 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gosele in view of Takagi and Yamauchi, and further in view of Gilleo et al. (US 5971253, of record).

p. **As to claim 3,** the rejection of claim 2 above is incorporated herein. Yamauchi discloses gold/gold bonding, however, Yamauchi does not teach forming a gold film on a surface of a base material (pads) having a hardness of 200 Hv or less, and after bonding, diffusing the gold into the base material. Gilleo et al. ("**Gilleo**") is drawn to microelectronic component mounting. Gilleo discloses (fig. 3) copper pads 56 (analogous to pads of Yamauchi) on the substrate/chip 54, having a coating 58 (i.e. film) formed from gold or other diffusion bondable metal, and a diffusion bonding material 40 in conjunction with sheet 22 (figs. 8-9a; col. 7, lines 24-40). The copper pads (base material) inherently have a hardness of 200 Hv or less. Diffusion bonding encompasses the gold film being diffused into the base material. Gilleo discloses that such bonding results in good connections even where the contacts of the chips and/or the pads of the substrate are slightly out of plane or of different heights (col. 7, lines 46-57). It would have been obvious to a person of ordinary skill in the art at the time of the

invention to implement the bonding technique of Gilleo in the modified method of Gosele because doing so results in good connections even where the contacts of the chips and/or the pads of the substrate are slightly out of plane or of different heights (Gilleo).

q. **As to claim 4,** both Yamauchi and Gilleo disclose the object being a semiconductor device. Gilleo discloses diffusing a gold film into the copper base material as explained in claim 3 above.

r. **As to claim 14,** Gosele as modified by Yamauchi and Gilleo above discloses that bonding portion is treated with said energy wave, a metal electrode is provided at a position facing said bonding surface of at least one of said objects to be bonded, forming a metal film. Yamauchi also discloses that sputtering the bonding surfaces in room-temperature bonding method of silicon wafers is known (¶ 3). It would have been obvious to form the metal film by sputtering in the bonding method of Gosele since the technique of sputtering was recognized as part of ordinary capabilities of one skilled in the art and would have only yielded predictable results at the time of the invention.

6. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gosele in view of Takagi and Yamauchi as applied to claim 6 above, and further in view of Linn et al. (US 5833758, of record).

s. **As to claim 7,** it is unclear whether Yamauchi discloses RF plasma generating power supply. However, Linn et al. (**"Linn"**, drawn to method for cleaning semiconductor wafers) discloses two-step RF plasma cleaning process

for wafers (col. 4, line 66 thru col. 3, line 10). It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide RF plasma generation similar to Linn in the modified method of Gosele in order remove contaminants from the surface and consequently improve bonding (Linn-abstract).

7. **Claims 9-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gosele in view of Takagi and Yamauchi as applied to claim 2 above, and in view of Linn et al. (US 5833758) and Usui et al. (US 2004/0140551).

t. **As to claim 9**, Yamauchi discloses plasma treatment of bonding portions, but fails to disclose a specific surface roughness of the bonding portions. However, **Linn** discloses that argon plasma cleaning (similar to Takagi and Yamauchi) roughens the surface and enhances the solderability to the substrate by increasing the surface of the bonding layer (col. 3, lines 12-15). It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide RF plasma generation similar to Linn in the method of Gosele in order to remove contaminants from the surface and consequently improve bonding (Linn-abstract). Linn is silent about surface roughness value. However, Usui et al. (**"Usui",** drawn to manufacturing semiconductor device) discloses surface processing a metal film to form a patterned interconnect line and to achieve surface roughness of 1 micron or less (i.e. greater than 120 nm), which effectively improves the high frequency performance (¶ 24; claim 14). The collective disclosures of Yamauchi, Linn and Usui teaches a bonding portion

having the surface roughness value 120 nm or more, and providing so would have been obvious to a person of ordinary skill in the art at the time of the invention in order to increase the surface area, improve bonding strength (Linn) and device performance (Usui).

u. **As to claim 10,** Yamauchi discloses the bonding apparatus including:

i. a head 7 (fig. 1) for holding one of the objects to be bonded;

ii. a stage 6 for holding the other object to be bonded; and

iii. a vertical drive mechanism for performing a position control with respect to at least one of said head and said stage in a direction substantially perpendicular to said bonding surface of said object to be bonded, and performing a pressing control (¶ 134).

iv. The vertical drive mechanism of Yamauchi is implicitly stopped at some point, when the bumps and pads are being bonded, thus it holds a constant height of the head 16 from said stage for a predetermined time. It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate the claimed elements in the modified method of Gosele in order to effectively perform surface-activated room-temperature bonding.

8. **Claims 13 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gosele in view of Takagi and Yamauchi as applied to claim 2 above, and further in view of Suga et al. (US 2003/0164396, of record).

v. **As to claim 13,** it is unclear whether Yamauchi discloses treating bonding portions with energy wave as claimed. However, **Suga** discloses a surface-activated bonding method, wherein in a chamber (7) having a reduced pressure, the bonding portions are treated with energy wave while bonding surfaces are not facing each other (in cleaning chamber 6), and thereafter, Suga discloses moving at least one of the objects (by conveying means 8 - ¶ 24-25) so that the bonding surfaces are contacted with each other in the chamber 7 (fig. 1). It would have been obvious to a person of ordinary skill in the art at the time of the invention to perform energy wave treatment similar to Suga in the modified method of Gosele since such is an art-recognized alternative approach and would have only yielded predictable results of activated bonding surfaces to one of ordinary skill in the art.

w. **As to claim 18,** Suga discloses that after said surface activation of said bonding portion, a vacuum state of a low- pressure chamber is replaced with filling gas, and said objects to be bonded are bonded in said filling gas to enclose said filling gas atmosphere in said space (figs. 1, 4-5; ¶ 36-39). The claim would have been obvious to an artisan for the same reasons set forth above.

9. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gosele in view of Takagi and Yamauchi as applied to claim 15 above, and further in view of Usui et al. (US 5686353).

x. **As to claim 16,** Yamauchi discloses bonding portion formed of gold but does not disclose the base material having hardness of 200 Hv or less, and a

gold plating having a thickness of 1 micron or more. However, such arrangement is well known in the art as shown by Usui. **Usui** (directed to semiconductor device mounting) discloses a gold film 402 having a thickness of about 1-10 micron on a copper base material 400 (fig. 5a; ¶ 79). The copper base material inherently has a hardness of 200 Hv or less. It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide the copper base and gold plating similar to Usui in the modified method of Gosele because doing so results in better adhesiveness and better plating (Usui- ¶ 79), thus improving bonding strength.

10. **Claims 11-12 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gosele in view of Takagi and Yamauchi as applied to claim 2 and 19 above, respectively, and further in view of Yagi et al. (US 5686353).

y. **As to claims 11-12,** none of the references above discloses leveling the bonding portion. However, such is well known in the art. Yagi et al. ("**Yagi**") discloses leveling step to obtain uniform height of each of the bumps, and adapting the height of each of the bumps to corresponding height of each of the electrodes on the substrate (col. 5, line 33 thru col. 6, line 20). It would have been obvious to a person of ordinary skill in the art at the time of the invention to perform leveling similar to Yagi in the method of Gosele in order to avoid the difficulties of non-uniformity and insufficient bonding strength (col. 3, lines 6-11).

z. **As to claim 20,** it is unclear whether Yamauchi discloses adjusting optimum positions of the objects to be bonded while the device is caused to

electrically function. **Yagi** discloses positioning the semiconductor device (i.e. chip) in relation to the substrate in a manner so as to transform the apex portion of each of the bumps and thus adapt height of each of the bumps to each of corresponding electrodes (col. 6, lines 4-12). Yagi further states that such provides extreme stability and accuracy, even if the electrodes have irregularity of thickness, or if the substrate has a warp. Yagi also discloses that the function test the electrical circuit is performed when the device is pressed against the substrate (col. 6, lines 22-28). It would have been obvious to a person of ordinary skill in the art at the time of the invention to perform positioning step of Yagi in the method of Gosele because it provides extreme stability and accuracy, even if the electrodes have irregularity of thickness, or if the substrate has a warp or undulation (col. 6, lines 13-21).

11. **Claims 52-53 and 59** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi (WO 2003/001858 A1) in view of Gilleo et al. (US 5971253, of record).

aa. **As to claim 52,** Yamauchi discloses gold/gold bonding, however, it is unclear whether Yamauchi discloses forming a gold film on a surface of a base material (pads 5) having a hardness of 200 Hv or less, and then diffusing the gold film into the base material. Gilleo et al. ("**Gilleo**") is drawn to microelectronic component mounting. Gilleo discloses copper pads 56 on the substrate 54 (fig. 3), being analogous to pads 5 of Yamauchi, having a coating 58 (i.e. film) formed from gold or other diffusion bondable metal, and a diffusion bonding material 40 in conjunction with sheet 22 (figs. 8-9a; col. 7, lines 24-40). The copper pads

(base material) inherently have a hardness of 200 Hv or less. Diffusion bonding encompasses the gold film being diffused into the base material. Gilleo discloses that such bonding results in good connections even where the contacts of the chips and/or the pads of the substrate are slightly out of plane or of different heights (col. 7, lines 46-57). It would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the bonding technique of Gilleo in the method of Yamauchi because doing so results in good connections even where the contacts of the chips and/or the pads of the substrate are slightly out of plane or of different heights (Gilleo).

bb. **As to claim 53,** the objects being bonded in Yamauchi include an IC chip, a semiconductor chip, a surface mounting part, or a wafer, and the bonding portions comprise a plurality of bumps (¶ 135). Yamauchi as modified by Gilleo above includes gold film diffused into the copper base material.

cc. **As to claim 59,** Yamauchi discloses that the bonding portion is formed in the shape of a contour, said bonding portion is surface-activated with said energy wave, and thereafter, said objects to be bonded are bonded together in a solid phase at room temperature, so that space surrounded in said shape of contour by said bonding portions is formed between said bonding surfaces of said objects to be bonded to enclose a predetermined atmosphere in said space.

Response to Amendment and Arguments

Applicant's arguments with respect to amended claims 2-3, 50 and new claims 51-59 have been fully considered but are moot in view of the new ground(s) of rejection set forth above. Specifically, Applicant's arguments against the Suga reference with respect to independent claims 2-3 and 50 are moot in light of new rejection including Gosele and Takagi. Gosele expressly discloses room-temperature bonding objects by crushing an adhering oxide layer between the bonding surfaces (fig. 1).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The rejections above rely on the references for all the teachings expressed in the text of the references and/or one of ordinary skill in the art would have reasonably

understood from the texts. Only specific portions of the texts have been pointed out to emphasize certain aspects of the prior art, however, each reference as a whole should be reviewed in responding to the rejection, since other sections of the same reference and/or various combinations of the cited references may be relied on in future rejections in view of amendments.

Applicant is reminded to specifically point out the support for any amendments made to the disclosure. See 37 C.F.R. 1.121; 37 C.F.R. Part 41.37; and MPEP 714.02.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEVANG PATEL whose telephone number is (571)270-3636. The examiner can normally be reached on Monday thru Thursday, 8:00 am to 5:30 pm, EST..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jessica Ward can be reached on 571-272-1223. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. P./
Examiner, Art Unit 1793

/Jessica L. Ward/
Supervisory Patent Examiner, Art Unit 1793